ABSTRACT OF THE DISCLOSURE

A system and method for effectuating the transfer of data blocks including a header block across a clock boundary between a first clock domain and a second clock domain. In one embodiment, a first circuit portion provides the data blocks including the header block to a second circuit portion. Control logic associated with the second circuit portion is operable to process the header block and generate in response to the header block a hint signal which is transferred via a synchronizer at least one data cycle prior to the transfer of the data blocks to a third circuit portion disposed in the second clock domain. A control block associated with the third circuit portion operates responsive to the hint signal to generate data transfer control signals for controlling the third circuit portion in order to control output of the data blocks in a particular ordered grouping.